REMARKS

Claims 1 – 34 are pending. Claims 1, 11, and 15 are amended. As discussed below, the claims are in condition for allowance. **But if after considering this response the Examiner does not agree that all of the claims are allowable, he is respectfully requested to schedule and conduct a telephone interview with the Applicants' attorney before issuing a subsequent Office Action.**

Allowed Claims

Claim 4 is allowed. The Applicants' agent thanks the Examiner for indicating allowance of claim 4.

Rejection of Claim 1 Under 35 U.S.C. § 112

The Applicants' agent thanks the Examiner for indicating the antecedent basis issue with claim 1. Claim 1 is amended herein to correct the cited deficiency.

Rejection of Claims 1-3 and 5-34 Under 35 U.S.C. § 103(a) Over Wong (U.S. Patent No. 6,282,627) In View of Ebeling (U.S. Patent No. 6,023,742)

Claim 1

Claim 1 as amended recites a plurality of pipeline units each coupled to the communication bus and each comprising a respective hardwired-pipeline circuit, including a first hardwired-pipeline circuit that operates synchronously with a first clock signal and at least one other hardwired-pipeline circuit that operates synchronously with a different clock signal.

For example, referring, e.g., to FIGS. 4-5 and paragraph [71] of U.S. Publication No. 2004/0136241, which the present application incorporates by reference, each pipeline unit 78 includes a pipeline circuit 80, which receives a respective CLOCK signal

(that is separate and distinct from the SYNC signal), and that may be unsynchronized with another CLOCK signal received by at least one of the other pipeline circuits 80.

In contrast, Wong does not disclose pipeline units comprising a respective hardwired-pipeline circuit synchronized to a respective clock signal that is unsynchronized with another clock signal to which at least one other hardwired-pipeline circuit is synchronized. Referring, *e.g.,* to FIG. 6, Wong's Datapath Program Units (DPUs) 621a and 621b are clocked by a common signal distributed via the Clock Distribution bus 609. Consequently, the clock signals respectively received by the DPUs are synchronized, not unsynchronized like the clock signals recited in claim 1.

Ebeling also does not disclose pipeline units comprising a respective hardwired-pipeline circuit, including a first hardwired-pipeline circuit that operates synchronously with a first clock signal and at least one other hardwired-pipeline circuit that operates synchronously with a different clock signal. While Ebeling's datapath 20 is apparently disclosed to operate asynchronously (column 9, lines 62-64), Ebeling apparently does not disclose hardwired-pipeline circuits that themselves operate from different, unsynchronized clocks.

Accordingly, Wong and Ebeling, alone and in combination, fail to disclose all the limitations of claim 1 and claim 1 is allowable over Wong and Ebeling.

Claims 2-3 and 5-10

These claims are patentable by virtue of their dependencies from claim 1.

Claim 11

Claim 11 is amended. Claim 11 recites a computing machine including a processor; a pipeline-accelerator configuration registry; a pipeline accelerator including a communication bus, a pipeline-bus interface coupled to the communication bus, and a plurality of pipeline units each coupled to the communication bus and each comprising a

respective hardwired-pipeline circuit disposed on a respective field-programmable-gate–array die; and a pipeline bus coupled to the processor, the registry, and the pipeline-bus interface of the pipeline accelerator.

In other words, claim 11 includes limitations similar to the limitations of claim 4, which has been allowed by the Examiner.

Neither Wong nor Ebeling disclose hardwired-pipeline circuits disposed on respective field-programmable-gate–array dies.

Accordingly, Wong and Ebeling fail to disclose all the limitations of claim 11 and claim 11 as amended is allowable over Wong and Ebeling.

Claims 12-13

These claims are patentable by virtue of their dependencies from claim 11.

Claim 15

Claim 15 is amended. Claim 15 is patentable for reasons similar to those given above in support of the patentability of claim 1.

Claims 16-22

These claims are patentable by virtue of their dependencies from claim 15.

Claim 23

Claim 23 recites a processor operable to retrieve program instructions via a program-instruction bus, and a pipeline accelerator inoperable to communicate directly with the program-instruction bus.

Referring, e.g., to FIG. 3 of the present patent application, the pipeline bus 50 is inoperable to communicate directly with the program-instruction bus (the bus between the processing unit 62 and the processing-unit memory 66).

In contrast, referring, e.g., to column 8, lines 56-65, unlike the claimed pipeline accelerator, Wong's reconfigurable logic is operable to communicate directly with an instruction-interface bus.

In contrast to the Examiner's assertion on p. 19, 3rd paragraph, the Applicants' agent disagrees that Ebeling includes the teaching missing from Wong, namely a pipeline accelerator inoperable to communicate directly with a program-instruction bus. In fact, the Examiner seems to indicate that Ebeling's instruction signals do converge with Ebeling's datapath in his statement "(See figure 8: The data path and instruction converge at one point)". The Applicant's agent agrees that the datapath and instructions converge at the closest structure in Ebeling apparently corresponding to "a plurality of pipeline units." This does not seem consistent with the Examiner's rejection, since claim 23 recites "a pipeline accelerator inoperable to communicate directly with the program-instruction bus," a condition apparently not met by Ebeling.

Referring to Ebeling's FIG. 8, the instruction signals/bus 16 is apparently operable to communicate directly with the configurable cells 26 via the control path 21. In particular, Ebeling discloses (at column 10, line 65 to column 11, line 55) that LUTs 220 receive instruction signals 16 and convert them into "dynamic control signals" 21. The dynamic control signals 21 are then "passed to the associated cell 26 as the data is pipelined down the data path 12." This appears to indicate that Ebeling's "pipeline accelerator" is operable to communicate directly with the program instruction bus.

The Applicant's agent maintains the previous argument that even if Ebeling's bus 16 is inoperable to communicate directly with the cells 26, there is no suggestion or motivation to combine the two architectures to obtain the computing machine recited in claim 23, nor is there a reasonable expectation of successfully obtaining a working architecture from such combination, and thus, the combination is improper.

Claim 24

Claim 24 is patentable for reasons similar to those recited above in support of the patentability of claim 23.

Claims 25-27

These claims are patentable by virtue of their dependencies from claim 24.

Claims 28 and 32-34

These claims are patentable by virtue of their dependencies on claim 11.

Claims 29-31

These claims are patentable by virtue of their dependencies on claim 1.

CONCLUSION

In light of the foregoing, claims 2-10, 12-14, and 16-34 as previously pending and claims 1, 11, and 15 as amended are in condition for full allowance, and that action is respectfully requested.

In the event additional fees are due as a result of this amendment, you are hereby authorized to charge such payment to Deposit Account No. 50-1464.

DATED this 5th day of July, 2007.

Respectfully submitted,

GRAYBEAL JACKSON HALEY LLP

Christopher A. Wiklof
Agent for the Applicant
Registration No. 37,560
155-108th Avenue N.E., Ste 350
Bellevue, WA 98004-5973
(425) 455-5575